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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Docket No: 29347/990488

PATENT APPLICATION TRANSMITTAL UNDER 37 C.F.R. 1.53

Box Patent Application
Commissioner for Patents
Washington, D.C. 20231

Sir:

Transmitted herewith for filing is the patent application of

Inventors: Gi-Young Jeun, O-Seob Jeun, Eun-Ho Lee and Seung-Won Lim

Title: SEMICONDUCTOR POWER MODULE HAVING AN ELECTRICALLY INSULATING HEAT SINK AND METHOD OF MANUFACTURING THE SAME

1. Type of Application

☒ This is a new application for a

☒ utility patent.

☐ design patent.

2. Application Papers Enclosed

1 Title Page

9 Pages of Specification (excluding Claims, Abstract, Drawings & Sequence Listing)

3 Pages of Claims

1 Page of Abstract

2 Sheets of Drawings (Figs. 1 to 3)

☒ Formal

☐ Informal

CERTIFICATION UNDER 37 CFR 1.10

I hereby certify that this Patent Application Transmittal and the documents referred to as enclosed therewith are being deposited with the United States Postal Service on **September 29, 2000**, in an envelope addressed to the Commissioner for Patents, Washington, D.C. 20231 utilizing the "Express Mail Post Office to Addressee" service of the United States Postal Service under Mailing Label No. EM099903919US.

Amanda White

Amanda White

3. **Declaration or Oath**

☐ Enclosed

☐ Executed by (check all applicable boxes)

☐ Inventor(s)

☐ Legal representative of inventor(s)
(37 CFR 1.42 or 1.43)

☐ Joint inventor or person showing a proprietary interest on behalf of inventor who refused to sign or cannot be reached

☐ The petition required by 37 CFR 1.47 and the statement required by 37 CFR 1.47 are enclosed.
See Item 5D below for fee.

☒ Not enclosed - the undersigned attorney or agent is authorized to file this application on behalf of the applicant(s). An executed declaration will follow.

4. **Additional Papers Enclosed**

☐ Preliminary Amendment

☐ Information Disclosure Statement

☐ Declaration of Biological Deposit

☐ Computer readable copy of sequence listing containing nucleotide and/or amino acid sequence

☐ Microfiche computer program

☐ Verified statement(s) claiming small entity status under 37 CFR 1.9 and 1.27

☐ Associate Power of Attorney

☐ Verified translation of a non-English patent application

☐ An assignment of the invention

☒ Return receipt postcard

☐ Other

5. **Priority Applications Under 35 USC 119**

Certified copies of applications from which priority under 35 USC 119 is claimed are listed below and

☒ are attached.

☐ will follow.

COUNTRY	APPLICATION NO.	FILED
Korea	99-42217	October 1, 1999

6. **Filing Fee Calculation (37 CFR 1.16)**

A. ☒ **Utility Application**

CLAIMS AS FILED - INCLUDING PRELIMINARY AMENDMENT (IF ANY)						
			SMALL ENTITY		OTHER THAN A SMALL ENTITY	
	NO. FILED	NO. EXTRA	RATE	FEE	RATE	FEE
BASIC FEE				$345.00		$690.00
TOTAL	18 -20	= -0-	X 9 =	$	X 18 =	-0-
INDEP.	2 - 3	= -0-	X 39 =	$	X 78 =	-0-
☐ First Presentation of Multiple Dependent Claim			+ 130 =	$	+ 260 =	-0-
			Filing Fee:	$	**OR**	$690.00

B. ☐ **Design Application ($155.00/$310.00)** Filing Fee: $ _____

C. ☐ **Plant Application ($240.00/$480.00)** Filing Fee: $ _____

D. **Other Fees**

☐ Recording Assignment [Fee -- **$40.00** per assignment] $ _____

☐ Petition fee for filing by other than all the inventors or person on behalf of the inventor where inventor refused to sign or cannot be reached [Fee -- **$130.00**] $ _____

☐ Other $ _____

Total Fees Enclosed $690.00

7. **Method of Payment of Fees**

☒ Enclosed check in the amount of: $690.00

☐ Charge Deposit Account No. 13-2855 in the amount of: $_____
A copy of this Transmittal is enclosed.

☐ Not enclosed

8. **Deposit Account and Refund Authorization**

The Commissioner is hereby authorized to charge any deficiency in the amount enclosed or any additional fees which may be required during the pendency of this application under 37 CFR 1.16 or 37 CFR 1.17 or under other applicable rules (except payment of issue fees), to Deposit Account No. 13-2855. A copy of this Transmittal is enclosed.

Please refund any overpayment to Marshall, O'Toole, Gerstein, Murray & Borun at the address below.

Respectfully submitted,

MARSHALL, O'TOOLE, GERSTEIN,
MURRAY & BORUN
6300 Sears Tower
233 South Wacker Drive
Chicago, Illinois 60606-6402
(312) 474-6300
(312) 474-0448 (Telefacsimile)

By: _____
James P. Zeller
Reg. No: 28,491

September 29, 2000

JOINT INVENTORS

"EXPRESS MAIL" mailing label No.
EM099903919US.
Date of Deposit: September 29, 2000
I hereby certify that this paper (or fee) is being deposited with the United States Postal Service "EXPRESS MAIL POST OFFICE TO ADDRESSEE" service under 37 CFR §1.10 on the date indicated above and is addressed to: Commissioner for Patents, Washington, D.C. 20231

Amanda White

APPLICATION FOR
UNITED STATES LETTERS PATENT

S P E C I F I C A T I O N

TO ALL WHOM IT MAY CONCERN:

Be it known that we, Gi-Young Jeun, a citizen of the Republic of Korea, of Samik Apt. 1826-304, Sang 1-dong, Wonmi-ku, Bucheon-city, Kyungki-do, Korea; O-Seob Jeun, a citizen of the Republic of Korea, of Daelim Apt. 2-308, Yeonheui 1-dong 700, Seodaemoon-ku, Seoul, Korea; Eun-Ho Lee, a citizen of the Republic of Korea, of Doosan Apt. 103, Sosabon 3-dong 403, Sosa-ku, Bucheon-city, Kyungki-do, Korea and Seung-Won Lim, a citizen of the Republic of Korea, of Rakwang Villa 302, Kwanyang 1-dong 1376-8, Dongan-ku, Anyang-city, Kyungki-do, Korea have invented a new and useful SEMICONDUCTOR POWER MODULE HAVING AN ELECTRICALLY INSULATING HEAT SINK AND METHOD OF MANUFACTURING THE SAME, of which the following is a specification.

PATENT APPLICATION
29347/990488

SEMICONDUCTOR POWER MODULE HAVING AN ELECTRICALLY INSULATING HEAT SINK AND METHOD OF MANUFACTURING THE SAME

BACKGROUND OF THE INVENTION

Field of the Invention

The invention relates generally to a semiconductor power module and, more particularly, the invention relates to a semiconductor power module having an electrically insulating heat sink.

Description of Related Technology

Generally speaking, a semiconductor power module is a packaged structure that typically includes a plurality of semiconductor die, which form a power circuit and a control circuit. These semiconductor die are mounted to die pads of a lead frame, which is molded together with a radiating metal plate (commonly referred to as a "heat sink") using epoxy resin.

As is well known, the power circuit within a semiconductor power module typically includes a power semiconductor element (e.g., a power transistor) that functions as a power switching device and the control circuit typically includes a driving element for driving (i.e., turning on and off) the power semiconductor element and a protection element that protects the power semiconductor element from damage due to over-current conditions, excessive temperatures, etc. In general, the power circuit is structured to radiate a substantial amount of heat because a significant amount of power is controlled and dissipated by the power semiconductor element. On the other hand, the control circuit typically draws small currents and does not dissipate an appreciable amount of power and, as a result, the control circuit typically does not have to be structured to radiate a substantial amount of heat.

As is also generally known, the management of heat generated within a conventional semiconductor power module is complicated by the fact that the

power circuit and the control circuit have significantly different heat dissipation requirements. Some developments have attempted to address the differential heat generation characteristics of the power circuit and control circuit within a semiconductor power module while attempting to provide a simple, cost-effective structure. For example, U.S. Patent No. 5,703,399 generally discloses a semiconductor power module having a lead frame, power and control circuits formed on the lead frame, an electrically conductive heat sink positioned adjacent to the power circuit and a sealer interposed between the heat sink and the lead frame that electrically insulates the heat sink from the lead frame and the circuit components mounted thereto. Unfortunately, the structure disclosed in U.S. Patent No. 5,703,399 requires a heat sink and a separate insulating layer and further requires that the heat sink be spaced in a uniform and stable manner to the control parasitic electrical effects that are produced as a result of using an electrically conductive material for the heat sink.

SUMMARY OF THE INVENTION

In accordance with one aspect of the invention, a semiconductor power module includes a lead frame having a first portion at a first level, a second portion surrounding the first portion at a second level, and a plurality of terminals connected to the second portion. The semiconductor power module may further include a power circuit mounted on a first surface of the first portion and an insulator having an electrically insulating property and thermal conductivity. The insulator may be adjacent to a second surface of the first portion of the lead frame. Additionally, the semiconductor power module may further include a sealer having an electrically insulating property that covers the power circuit.

In accordance with another aspect of the invention, a method of manufacturing a semiconductor power module having a lead frame with a first portion at a first level and a second portion surrounding the first portion at a

second level includes the steps of die-bonding a power circuit onto a first surface of the first portion of the lead frame and wire bonding electrodes of the power circuit to corresponding portions of the lead frame. The method may further include the steps of molding the lead frame and the power circuit with a sealer and adhering an insulator with thermal conductivity and an electrically insulating property onto a second surface of the first portion.

The invention itself, together with further objectives and attendant advantages, will best be understood by reference to the following detailed description, taken in conjunction with the accompanying drawings and the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is an exemplary cross-sectional diagrammatic view of a semiconductor power module according to one embodiment of the invention;

Fig. 2 is and exemplary plan view of a lead frame that may be used within the semiconductor power module shown in Fig. 1; and

Fig. 3 is an exemplary cross-sectional diagrammatic view of a semiconductor power module according to another embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

The semiconductor power module described herein uses an electrically insulating heat sink to dissipate the heat generated by a power circuit within the semiconductor power module. Generally speaking, the semiconductor power module described herein includes a power circuit that is mounted to a lead frame and which is covered with an electrically insulating sealant to protect the circuit from environmental damage. The semiconductor power module described herein also includes an electrically insulating heat sink that is adjacent to the lead frame and which dissipates heat generated by the power circuit. Because the heat sink is made of an electrically insulating

material, a separate insulating layer is not required between the heat sink and the lead frame and, in some embodiments, the heat sink may directly contact the lead frame. Furthermore, the electrically insulating heat sink of the semiconductor power module described herein does not produce the undesirable parasitic electrical effects (e.g., parasitic capacitance, etc.) such as those which are caused by the electrically conductive heat sinks used within conventional semiconductor power modules.

Fig. 1 is an exemplary cross-sectional diagrammatic view of a semiconductor power module 100 according to one embodiment of the invention. As shown in Fig. 1, the semiconductor power module 100 includes a centrally positioned power circuit 10, a heat detection circuit 20 that detects the loss heat produced by the power circuit 10, and a peripherally positioned control circuit 30 that controls the operation of the power circuit 10.

The power circuit 10 includes a power semiconductor element 11 that performs a switching operation. The power semiconductor element 11 typically includes emitter, collector and gate electrodes and may, for example, be a metal oxide semiconductor field effect transistor (MOSFET) or any other suitable switching device. In operation, the power semiconductor element 11 switches a flow of current from the collector electrode to the emitter electrode based on a signal that is applied to the gate electrode. The power circuit 10 may further include a protection circuit (not shown) that prevents the power semiconductor element 11 from being damaged by excessive reverse currents.

The heat detection circuit 20 includes a thermistor element 21, which is used by the heat detection circuit 20 to detect the loss heat produced by the power semiconductor element 11. The heat detection circuit 20 monitors the operational temperature of the power semiconductor element 11 (and the power circuit 10) to prevent the power circuit 10 from being damaged as a result of an over-temperature condition.

The control circuit 30 is electrically coupled to the power circuit 10 and includes an integrated circuit element 31. The control circuit 30 may further

include a resistance element and/or a capacitive element (neither of which are shown).

The power semiconductor element 11, the thermistor element 21 and the integrated circuit element 31 are all mounted to a lead frame 40, which is formed from a material having a high thermal conductivity such as copper. The power semiconductor element 11, the thermistor element 21 and the integrated circuit element 31 are electrically coupled to suitable portions of the lead frame 40 via bonding wires 50, which may, for example, be made of gold, aluminum or any other suitable material.

A sealer 60 covers the lead frame 40, the power semiconductor element 11, the thermistor 21, the integrated circuit element 31 and the bonding wires 50. The sealer 60 provides resistance to environmental elements such as moisture, vibration, corrosive gases and liquids, etc. Additionally, the sealer 60 provides a good electrical insulation property and a good thermal conductivity.

An insulator 70 may be formed at the bottom surface of the lead frame 40, which is opposite to surface on which the power semiconductor element 11 is mounted. The insulator 70 is made of a material having a good thermal conductivity and a good electrical insulation property. For example, materials such as Al_2O_3, AlN and BeO may be used to form the insulator 70. Of course, other materials having good thermal conductivity and electrical insulation properties may be used instead without departing from the scope and spirit of the invention. Because the insulator 70 has good electrical insulation properties, the insulator 70 may directly contact the lead frame 40 without causing electrical shorting or undesirable parasitic effects such as those which are typically caused by conventional electrically conductive heat sinks. However, in some applications it may be desirable to allow the sealer 60 to completely encapsulate the semiconductor power module 100 such that the sealer 60 covers the bottom surface of the lead frame 40. In that case, the insulator 70 may be mounted directly to the sealer 60 without concern for uniform and/or stable spacing of the insulator 70 from the lead frame 40

because the insulator 70 does not introduce the parasitic electrical effects such as those introduced by the electrically conductive heat sinks which are used within conventional semiconductor power modules. Thus, the semiconductor power module described herein does not require a separate heat sink and insulator as do conventional semiconductor power modules because the insulator 70 functions as a heat sink.

Fig. 2 is an exemplary plan view of the lead frame 40 that may be used within the semiconductor power module 100 shown in Fig. 1. As shown in Fig. 2, the lead frame 40 has a centrally positioned first portion 41, which is indicated by a dashed line, and a second portion 42 surrounding the first portion 41 that is indicated by a broad solid line. The first portion 41 of the lead frame 40 includes a power pad 411, upon which the power semiconductor element 11 is mounted, and a heat detection pad 211, upon which the thermistor element 21 is mounted. Additionally, the second portion 42 of the lead frame 40 includes a control pad 311, upon which the integrated circuit element 31 is mounted.

The lead frame 40 further includes an interconnection wiring pattern that interconnects the power circuit 10, the heat detection circuit 20 and the control circuit 30 via the wires 50. This interconnection wiring pattern also interconnects the power circuit 10, the heat detection circuit 20 and the control circuit 30 to external terminals 43 (which are part of the second portion 42) to enable the input or output of electrical signals through the terminals 43. Those of ordinary skill in the art will recognize that the interconnection pattern formed by the lead frame 40 may be varied to suit the desired circuit function within any particular application.

The lead frame 40 further includes a plurality of opening portions 401 that may be used to fixture the position of the lead frame 40 during assembly of the semiconductor power module 100. As shown in Fig. 2, the terminals 43 are connected to the pads 211, 311 and 411 to form a unitary structure via a connection part 45. After the molding process is completed, as shown in Fig.

1, the connection part 45 is cut off so that the terminals 43 are separated from each another.

Preferably, the lead frame 40 is made of a copper material or a copper-based alloy material. Also preferably, the lead frame 40 is surface treated to prevent the lead frame 40 from oxidizing. For example, the surface of the lead frame 40 may be electroplated using nickel or any other suitable plating material. In some embodiments it may be desirable to provide additional electroplating material thickness on portions of the lead frame 40 that are used as mounting pads for semiconductor chips.

Referring again to Fig. 1, the lead frame 40 is bent at an obtuse angle about a bent portion 44 so that the first portion 41 and the second portion 42 are at different levels and so that the first portion 41 is closer to the insulator 70 than the second portion 42. With the structure shown in Fig. 1, the loss heat produced by the power semiconductor element 11 (which is mounted on the first portion 41) is effectively dissipated through the insulator 70. The bent portion 44 of the lead frame 40 is formed with a width smaller than that of the first and second portions 41 and 42 and the second portion 42 of the lead frame 40 connected to the terminals 43 is bent in a direction opposite to the insulator 70. Thus, when mounting the semiconductor power module 100 to an application device having an unlimited radiating plate, the terminals 43 may be spaced sufficiently apart a predetermined distance from the unlimited radiating plate while preventing contact therebetween.

The heat detection circuit 20 may be formed on the second portion 42 of the lead frame 40 instead of on the first portion 41. Alternatively, the heat detection circuit 20 may be dispensed with altogether. Further, the control circuit 30 may be formed on the first portion 41 of the lead frame 40 while maintaining constant performance characteristics by making appropriate modifications to the semiconductor power module 100.

In manufacturing the semiconductor power module 100 shown in Fig. 1, the lead frame 40 may be fabricated using a stamping operation. A solder

preform (e.g., solder paste) may then be formed on the lead frame 40 and chips such as the power semiconductor element 11, the thermistor element 21 and the integrated circuit element 31 are placed onto the pads 211, 311, and 411. The composition of the solder preform is selected and controlled so that the preform material can be melted at a temperature of about 300 °C. The power semiconductor element 11 is oriented on the first portion 41 of the lead frame 40 near to the outer periphery of the semiconductor power module 100 so that the loss heat generated by the semiconductor element 11 may be more easily dissipated.

After the various die used within the semiconductor power module 100 have been mounted to the lead frame 40, the electrodes of the semiconductor element 11, the thermistor 21 and the integrated circuit element 31 are wire-bonded to suitable portions of the wiring interconnection pattern formed by the lead frame 40. This wire-bonding operation may be any known process such as, for example, wedge or ball bonding, using any suitable wire material, such as, for example, aluminum or gold.

Following the die-bonding operation, the lead frame with chips mounted thereto is covered with an epoxy molding compound to form the sealer 60. Preferably, the epoxy is cured at about 160 °C to 170 °C, however, other temperatures and curing conditions (e.g., using ultraviolet cured epoxy) may be used without departing from the scope of the invention.

After application of the sealer 60, the insulator 70, which may be sheet shaped, is adhered adjacent to the bottom surface of the lead frame 40 near the first portion 41. In operation, the insulator 70 functions as a heat sink and effectively dissipates the loss heat generated by the power semiconductor element 11. Additionally, the insulator 70 functions to evenly distribute stresses from external impacts to prevent the occurrence of cracks and other types of damage to the power semiconductor module 100. In some embodiments, the insulator 70 may be adhered to the lead frame 40 using an adhesive containing a filler such as Al_2O_3, AlN, or BeO, which provide good

electrical insulation properties and good thermal conductivity. Further, the insulator 70 may be bent to prevent deflection transformation thereof caused by adherence of other materials thereto. In other embodiments, the sealer 60 and the insulator 70 may have rings or grooves that enable the insulator 70 to be detachably mounted (e.g., pressed on, threaded on, etc.) to the semiconductor power module 100.

Fig. 3 is an exemplary cross-sectional diagrammatic view of a power module according to another embodiment of the invention. The power module shown in Fig. 3 includes many of the same or similar components that are used in the embodiment shown in Fig. 1. However, in the power module shown in Fig. 3, the heat detection circuit 20 has been omitted and the control circuit 30 is formed on the first portion 41 of the lead frame 40.

A range of changes and modifications can be made to the preferred embodiment described above. The foregoing detailed description should be regarded as illustrative rather than limiting and the following claims, including all equivalents, are intended to define the scope of the invention.

CLAIMS

What is claimed is:

1. A semiconductor power module, comprising:

a lead frame having a first portion at a first level, a second portion surrounding the first portion at a second level, and a plurality of terminals connected to the second portion;

a power circuit mounted on a first surface of the first portion;

an insulator having an electrically insulating property and thermal conductivity, wherein the insulator is adjacent to a second surface of the first portion; and

a sealer having an electrically insulating property that covers the power circuit.

2. The semiconductor power module of claim 1, wherein the first portion of the lead frame is centrally positioned within the lead frame.

3. The semiconductor power module of claim 1, wherein the power circuit includes a power semiconductor element.

4. The semiconductor power module of claim 1, wherein the first surface of the first portion is a top surface and wherein the second surface of the first portion is a bottom surface.

5. The semiconductor power module of claim 1, further comprising a control circuit that drives the power circuit.

6. The semiconductor power module of claim 1, further comprising a heat detection circuit that detects the heat produced by the power circuit.

7. The semiconductor power module of claim 1, wherein the insulator directly contacts the second surface of the lead frame.

8. The semiconductor power module of claim 1, wherein the insulator is adhered to at least one of the lead frame and the sealer with an adhesive.

9. The semiconductor power module of claim 8, wherein the adhesive contains a filler that includes at least one compound selected from the group consisting of Al_2O_3, AlN and BeO.

10. The semiconductor power module of claim 1, wherein the insulator and the sealer each have grooves or rings and wherein the insulator and the sealer are connected to each other by means of the grooves or the rings.

11. The semiconductor power module of claim 1, wherein the insulator is sheet-shaped and comprises at least one compound selected from the group consisting of Al_2O_3, AlN, and BeO.

12. A method of manufacturing a semiconductor power module having a lead frame with a first portion at a first level and a second portion surrounding the first portion at a second level, the method comprising the steps of:

die-bonding a power circuit onto a first surface of the first portion of the lead frame;

wire bonding electrodes of the power circuit to the lead frame;

molding the lead frame and the power circuit with a sealer; and

adhering an insulator with thermal conductivity and an electrically insulating property onto a second surface of the first portion.

13. The method of claim 12, further comprising the step of die-bonding a heat detection circuit onto the lead frame.

14. The method of claim 12, wherein the step of adhering the insulator onto the second surface of the first portion includes the step of adhering the insulator directly to the first portion of the lead frame.

15. The method of claim 12, comprising the step of adhering the insulator onto the second surface of the first portion with an adhesive.

16. The method of claim 15, wherein the adhesive contains at least one compound selected from the group consisting of Al_2O_3, AlN and BeO.

17. The method of claim 12, wherein the insulator and the sealer each have grooves or rings and wherein the insulator and the sealer are connected to each other by means of the grooves or the rings.

18. The method of claim 12, wherein the insulator is sheet-shaped and comprises at least one compound selected from the group consisting of Al_2O_3, AlN, and BeO.

SEMICONDUCTOR POWER MODULE HAVING AN ELECTRICALLY INSULATING HEAT SINK AND METHOD OF MANUFACTURING THE SAME

ABSTRACT OF THE DISCLOSURE

A semiconductor power module includes a lead frame having a first portion at a first level, a second portion surrounding the first portion at a second level, and a plurality of terminals connected to the second portion. The semiconductor power module further includes a power circuit mounted on a first surface of the first portion and an insulator having an electrically insulating property and thermal conductivity. The insulator is adjacent to a second surface of the first portion of the lead frame. The semiconductor power module further includes a sealer having an electrically insulating property that covers the power circuit and the control circuit.

FIG. 1

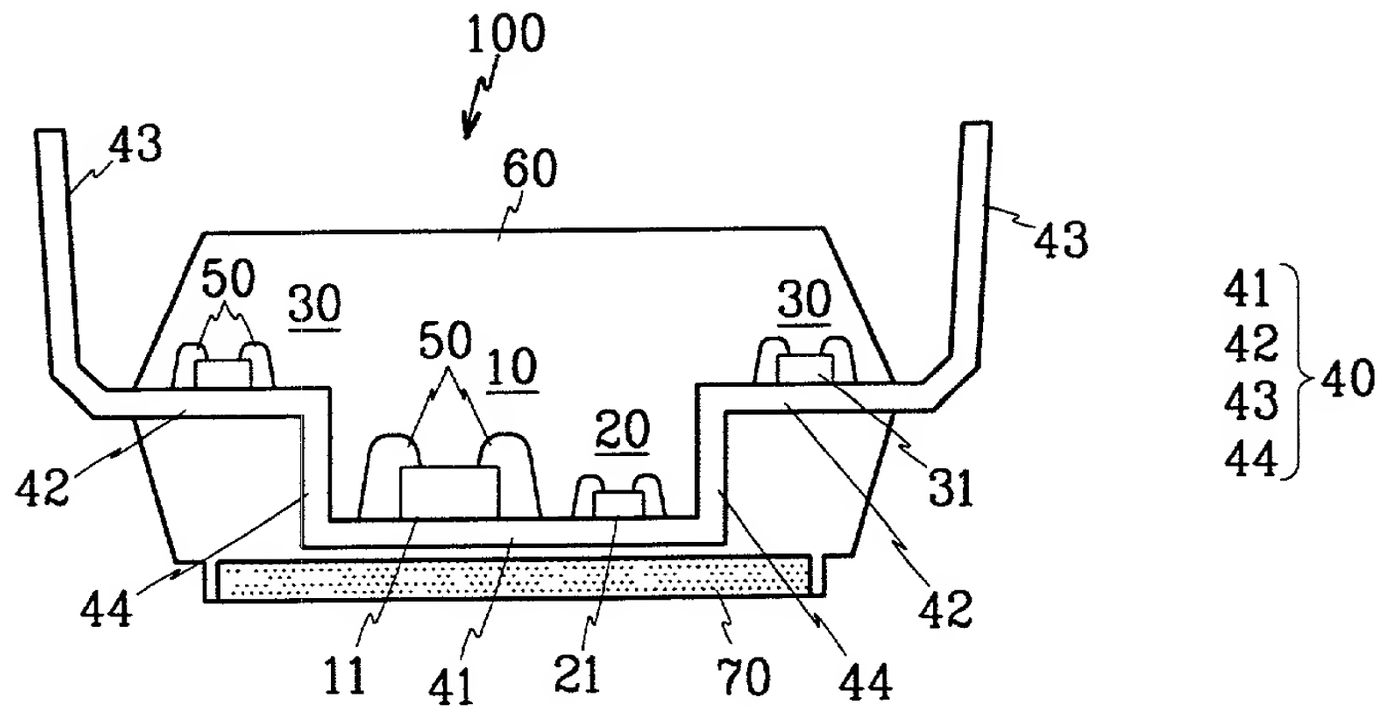
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FIG. 3

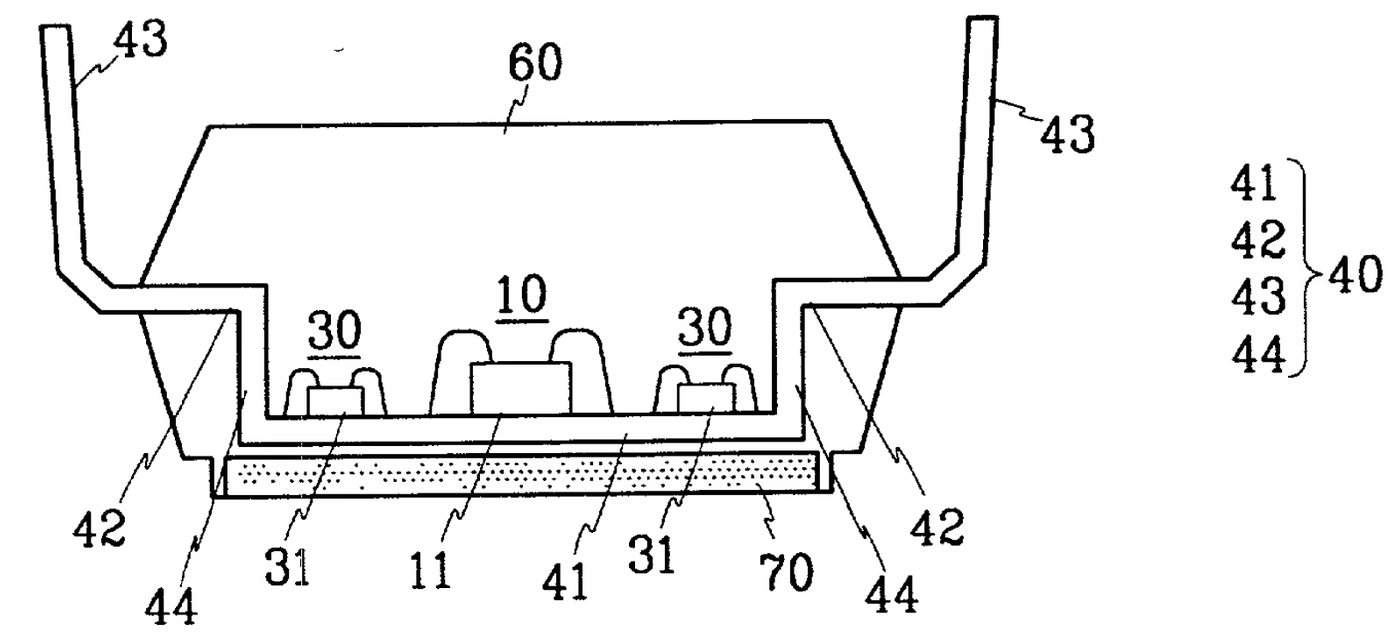
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FIG. 2